

FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO



**Development of a reconfigurable
multi-protocol verification environment
using UVM methodology**

Pedro Araujo

DISSERTATION
PROGRESS REPORT 2

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

Teacher supervisor: José Carlos Alves

Company supervisors: Luis Cruz and Domingos Terra

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Chapter 1

Report

Work done:

- Study of the existing UVM verification environment
- Study of some fundamental concepts about digital verification
- Research of theoretical concepts to be included in the final document

