FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Development of a reconfigurable multi-protocol verification environment using UVM methodology

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DISSERTATION
PROGRESS REPORT 3

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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Chapter 1

Report

Work done:

- Completion of the UVM guide for beginners
- Presentation of possible approaches to a generic verification environment
- Start of the experimentation of these approaches by developing a verification envinroment for an I2C bus

Difficulties:

- Due to the study of some missing concepts about verification, the project is delayed about two weeks in relation ot the original planning. But as the final deadline is 30th of June and the project was planned to be finished in the first week of June, this delay shouldn't be very critical.