FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Development of a reconfigurable multi-protocol verification environment using UVM methodology

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DISSERTATION
PROGRESS REPORT 1

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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Chapter 1

Report

Work done:

- Writing of the Preliminary Report with some research about the evolution of verification methodologies
- Completed the study and research of the UVM methodology
- Started to study and documenting an existing verification environment used by the company
- Started to structure a guide about UVM for beginners to the methodology

Difficulties:

- Although the most essential features and structure of UVM is apprehended, there are fundamental concepts about verification of digital designs that are missing and that are important for the realization of this thesis. This will need to be overcomed with some study about verification concepts in the next few weeks.